1.counter verilog code

MODULE CODE

module counter\_bcd(clk,reset,cout);

input clk,reset;

output reg [3:0]cout;

always@(posedge clk)

begin

if(reset==1'b1 | cout>=4'd9)

cout=4'b0000;

else

cout=cout+1;

end

endmodule

AND\_XOR code

MODULE CODE

module and\_xor\_generator(fun\_s,a,b,y,z);

input fun\_s,a,b;

output reg y,z;

always@(a,b,fun\_s)

begin

if(fun\_s==0)

y=a&b;

else

z=a^b;

end

endmodule

TEST BENCH